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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/714,105	11/14/2003	Anthony Correale JR.	RPS920030130US1	1935

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IBM CORPORATION
PO BOX 12195
DEPT YXSA, BLDG 002
RESEARCH TRIANGLE PARK, NC 27709

EXAMINER	
HEIN, GREGORY P	
ART UNIT	**PAPER NUMBER**
2188	

DATE MAILED: 01/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/714,105	CORREALE ET AL.	
	Examiner	Art Unit	
	Gregory P. Hein	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 10 and 12 - 14* is/are rejected.

7)☐ Claim(s) *11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 8 is objected to because of the following informalities: the sentence "a clock signal circuit for supplying clock signals to one or both of said ways response to an access mode signal" is missing a preposition to make the sentence more coherent. Appropriate correction is required.

Specification

1. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: Claim 1, line 5 recites subject matter "an address circuit." This subject matter does not appear in the specification. Claim 2, line 3 cites the subject matter "a tag array." This subject matter doe not appear in the specification.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: At least reference numbers 17 and 18 do not appear in the specification. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures

appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the address circuit must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner,

the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 2 recites the limitation "said sets" in line 5 and 7. There is insufficient antecedent basis for this limitation in the claim.

6. Claim 4 recites the limitation "said sets" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Double Patenting

7. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

8. Claims 1 – 3 and 5 – 10 rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 4 – 5, 9, 13 – 15, 17, and 19 - 20 of U.S. Patent No. 6,961,276 (Atallah et al). Although the conflicting claims are not identical, they are not patentably distinct from each other because the variations between the claims would have been obvious to one of ordinary skill in the art at the time of the invention.

9. Claim 1 is mapped with the corresponding claim limitation of the patent 6,961,276 in the table below for illustrative purposes.

U.S. Application No. 10/714,105	U.S. Patent No. 6961276
1. A system for accessing a two way associative data cache having first and second ways	14. A tag random access memory (RAM) including a plurality of memory cells and a plurality of data ways
a clock circuit for selectively applying clock pulses to one or to both ways of said two way associative cache in response to a mode access signal	15. The controller is configured to selectively adapt the latency ... based at least in part on a timing signal
an address circuit connected to simultaneously apply an address to each of said sets of said two way associative cache	14. At least one decoder operatively coupled to the memory cells ... the at least one decoder being configurable for receiving the input address and for accessing one or more of the memory

	cells in response thereto
an output multiplexer for selecting data from one of said sets of said associative cache in response to a select signal identifying one of said ways of said associative cache	20. At least one multiplexer operatively coupled to at least a portion of the plurality of sense amplifiers, the multiplexer including at least one control input for receiving a select signal.

As per claim 2, Atallah claims:

A tag array connected to be addressed by said address circuit for storing first and second sets of tag signals corresponding to a corresponding set of data stored in said first and second ways (Atallah claim 14 claims "a tag random access memory (RAM) including a plurality of memory cells and a plurality of ways"); and

first and second comparators connected to compare first and second output data from said tag array with tag data derived from said address thereby identifying one of said ways of said associative caches containing data to be read, said one comparator generating a select signal for said output multiplexer (Atallah claim 14 claims "a plurality of comparators each of the comparators including a first input coupled to a corresponding one of the data ways, a second input for receiving at least a portion of an input address").

As per claim 3, Atallah claims:

The control signal applied clock pulses to both ways of said associated cache when the access time for reading said data from one of said sets is less than a

predetermined amount (Atallah claim 19 claims "the controller dynamically changes the latency of the cache memory circuit in response to at least one characteristic associated with the cache memory circuit.")

As per claim 5, Atallah claims:

The clock circuit receives data from said comparator identifying which of said ways of said associative cache is to be clocked (Atallah claim 17 claims "each of at least a portion of the comparators are configured to generate a control signal at its output that is at least initially set to enable a sense amplifier.")

As per claim 6, Atallah claims:

The clock circuit receives an access mode signal which indicates that both of said sets of associative cache are to be clocked simultaneously (Atallah claim 15 claims "the controller is configured to selectively adapt the latency of the cache memory circuit by at least one of enabling and disabling the sense amplifiers")

As per claim 8, Atallah claims:

A system for accessing a data cache having at least two ways for storing data at the same addresses (Atallah claim 13 claims "a plurality of data ways"), comprising:

a first and second tag memory for storing ftrst and second sets of tags identifying data stored in each of said ways (Atallah claim 13 claims "at least one tag random access memory");

a translation device for determining from a system address a tag identifying one of said ways (Atallah claim 13 claims "each of the comparators including ... a second input for receiving at least a portion of the input address");

a first comparator for comparing tags in said address with a tag stored in said first tag memory;

a second comparator for comparing a tag in said address with a tag stored in said second tag memory (Atallah claim 13 claims "each of the comparators including a first input coupled to a corresponding one of the data ways, a second input for receiving at least a portion of the input address");

a multiplexer for selecting output data from one of said ways in response to a signal from one of said first and second comparators (Atallah claim 5 claims "at least one multiplexer operatively coupled to at least a portion of the plurality of sense amplifiers, the multiplexer including at least one control input for receiving a select signal"; and

a clock signal circuit for supplying clock signals to one or both of said ways response to an access mode signal (Atallah claim 1 claims "a plurality of sense amplifiers operatively coupled to the memory cells, the sense amplifiers being configurable for determining a logical state of one or more of the memory cells; and a controller coupled to at least a portion of the sense amplifiers, the controller being configurable for selectively operating in at least one of a first mode and a second mode, wherein in the first mode the controller enables one of the sense amplifiers corresponding to the input address and disables the sense amplifiers not corresponding to the input address, and in the second mode the controller enables substantially all of the sense amplifiers.")

As per claim 9, Atallah claims:

The access mode signal has a first state which represents a power efficiency mode of operation (Atallah claim 4 claims "the first mode comprises a power-saving mode").

As per claim 10, Atallah claims:

The access mode signal has a second state which represents a high access speed for said cache (Atallah claim 4 claims "the second mode comprises a low-latency mode").

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

11. Claims 1 – 14 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Pre-Grant Publication 2005/0063211 (Atallah et al).

The applied reference has a common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in

the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

As per claim 1, Atallah teaches accessing a two-way associative data cache (Atallah ¶20 lines 5 – 8 Atallah discloses that the invention is not limited to any particular number of associative ways including two-way associative caches.)

Atallah teaches a clock circuit for selectively applying clock pulses to the multiple cache ways responsive to an access mode signal (Atallah ¶40 lines 3 – 8).

Atallah ¶25 lines 3 - 7 teaches an address circuit connected to simultaneously apply an address to way.

Attallah ¶26 lines 14 – 20 teach an output multiplexer selecting data from one of the ways responsive to a select signal.

As per claim 2, Atallah teaches a tag array to be addressed by address circuitry storing tag information corresponding to data stored in cache ways (Atallah ¶23)

Atallah ¶21 lines 5 – 15 teach comparators connected to tag arrays and data from the effective address thus identifying one of the cache ways for data output selection.

As per claim 3, Atallah teaches a control signal applied clock pulses to the cache ways then the access time is less than a predetermined amount (Atallah ¶18 lines 1 – 5 teach accessing all of the ways simultaneously and lines 14 – 18 teach operating in this mode depending on the clock frequency. Atallah ¶40 lines 3 – 8 teach the mode is responsive to the timing signal SAE.)

As per claim 5, Atallah discloses the clock circuit receiving data from the comparators identifying which way of the cache to be clocked (Atallah ¶26 lines 14 – 20 disclose the enable circuitry receiving as input the output of the comparators. Enable circuitry also receives as input the SA_TIM signal derived from the system clock as disclosed in Atallah ¶45 lines 8 – 16.)

As per claim 6, Atallah teaches a clock circuit receiving an access mode signal indicating the cache way access mode (Atallah ¶40 discloses lines 3 – 8 and ¶44)

As per claim 7, Atallah teaches the access signal is selected based on need for power conservation by means of only a single way access or a need to increase access speed by way of simultaneously accessing all cache ways (Atallah ¶40 lines 3 – 8 disclose that the operational mode is responsive to signal SAE. Atallah ¶41 discloses multiple methodologies for selecting SAE including hardware failure, software demands, circuit layout, and clock frequency.)

As per claim 8, Atallah discloses a multiple-way cache (Atallah ¶20 line 6 "nor is it limited to a particular number of ways")

Atallah teaches tag memories for storing tags identifying data stored in each of the cache ways (Atallah ¶21 discloses a tag RAM with output comparators associated with each of the cache ways.)

Atallah teaches a translation device for determining from a system address a tag identifying a cache way (Atallah ¶38 lines 8 – 11 The tag RAM translates the effective address. The comparators then determine from the system address the corresponding cache way.)

Atallah teaches comparators to compare the system address to tags stored in the tag memory (Atallah ¶24 lines 5 – 10.)

Atallah teaches a multiplexer controlled by a signal from the comparators for selecting output data from one of the cache ways (Atallah ¶26 lines 14 – 19.)

Atallah teaches a clock signal circuit for supplying clock signals to one or multiple ways (Atallah ¶40 lines 3 – 8 The SAE signal determines the access mode.)

As per claim 9, Atallah teaches an access mode signal that has a first state representing a power efficient mode (Atallah ¶40 lines 8 –11.)

As per claim 10, Atallah teaches an access mode signal that has a second state representing an improved access time mode (Atallah ¶40 lines 11 – 14.)

As per claim 12, Atallah teaches a method for accessing a set associative data cache comprising at least two ways (Atallah ¶23 line 6 "nor is it limited to a particular number of ways"),

Atallah discloses addressing cache ways with identical line index addresses derived from an effective address (Atallah ¶23 discloses the cache data RAM are coupled to the line index of the effective index.)

Atallah discloses addressing tag memories with a line index address and determining whether said first or second tag memories produce a tag identical to the tag taken from the effective address (Atallah ¶23 discloses that the line index of the effective address is coupled to both the cache data RAM and the tag memory array. Atallah ¶38 lines 8 – 11 The comparators determine which way holds the data corresponding to the tag memory data.)

Atallah discloses reading data from one of the cache ways in response to a first state of an access signal, and reading data from all cache ways when said access signal has a second state (Atallah ¶40 lines 8 – 14).

As per claim 13, Atallah teaches a method for accessing a set associative data cache wherein a first state of an access signal is selected when said data cache is read in a power conserving mode, and a second state of an access signal is selected when said data cache is operated in a high speed access mode (Atallah ¶40 lines 8 - 14).

As per claim 14, Atallah discloses 14 an access mode signal controls a clock circuit that applies a clocking signal to a first way in said first state, and applies clocking signals to all ways when the access mode signal is in a second state (Atallah ¶42 lines 1 – 14 and ¶43 lines 8 – 16 describe the enable circuitry. The SA_TIM signal is generated based on several characteristics of the circuit in addition to the system clock. The SAE signal is the access mode signal. Together and in addition to several other test signals these signals control the timing of the access to the cache data RAM and the mode, either high speed or low power, in which the cache data RAM is accessed.)

Allowable Subject Matter

12. Claim 11 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gregory P. Hein whose telephone number is 571-272-4180. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mano Padmanabhan 1/9/06

Gregory Hein
01/04/2006

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER